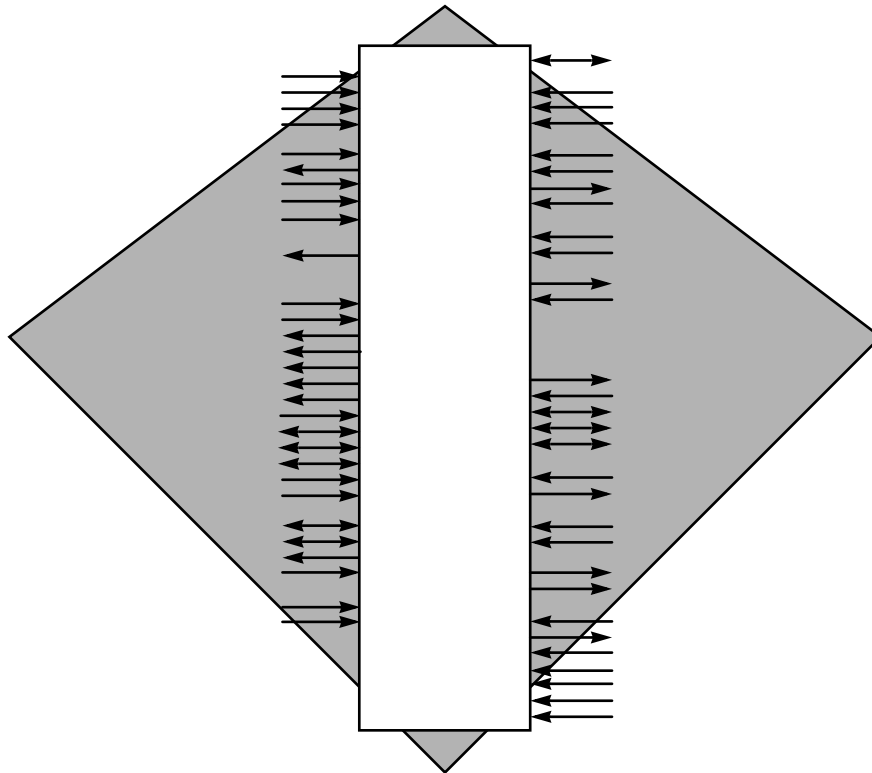


## SECTION 2

# SIGNAL/CONNECTION DESCRIPTION



# **Freescale Semiconductor, Inc.**

## **Signal/Connection Description**

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|      |                                                 |      |
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## 2.1 INTRODUCTION

The input and output signals of the DSP56602 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-13**, each table row describes the signal or signals present on a pin.

The DSP56602 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

**Table 2-1** Functional Group Signal Allocations

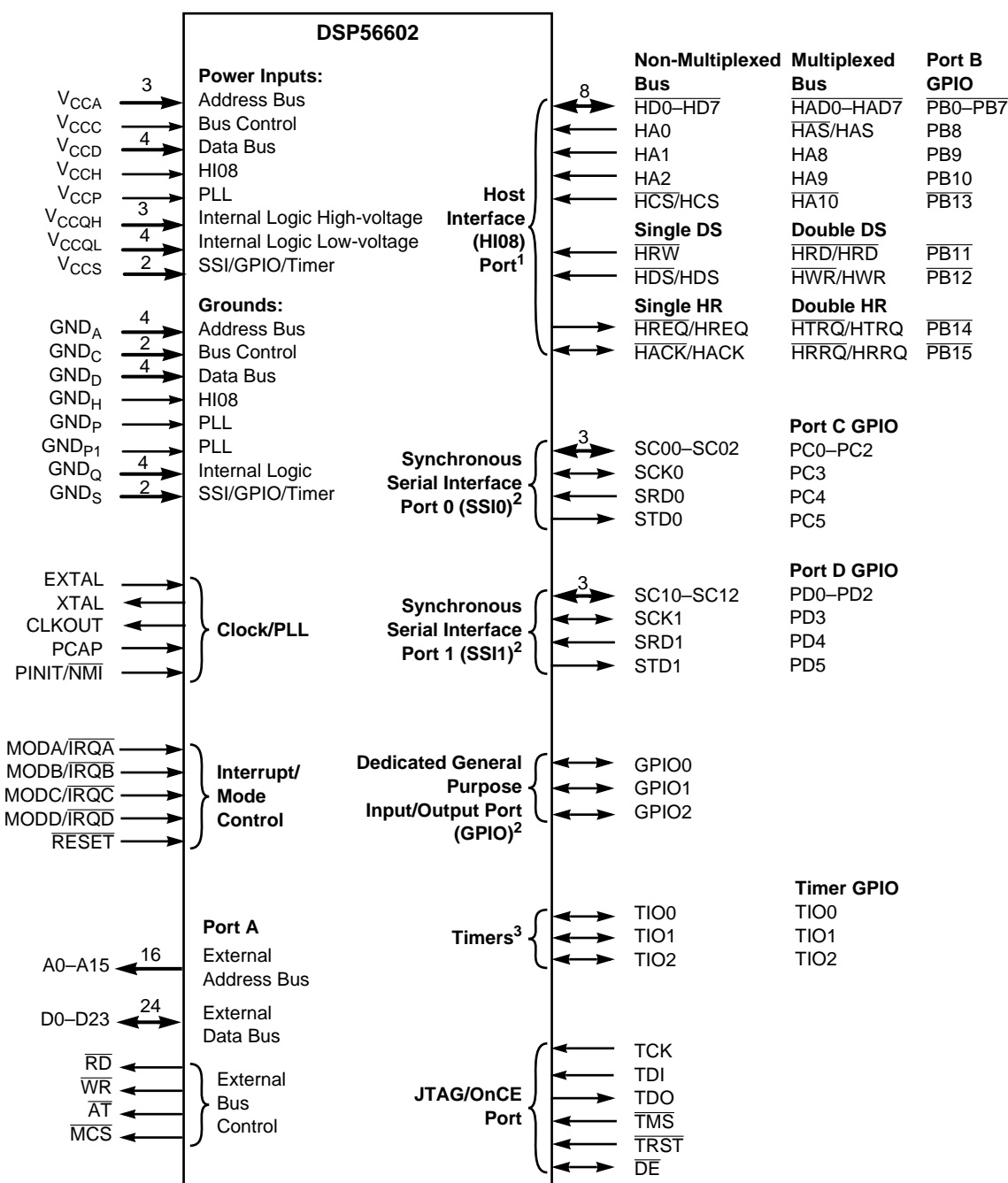
| Functional Group                                       |               | Number of Signals | Detailed Description |
|--------------------------------------------------------|---------------|-------------------|----------------------|
| Power ( $V_{CC}$ )                                     |               | 19                | <b>Table 2-2</b>     |
| Ground (GND)                                           |               | 19                | <b>Table 2-3</b>     |
| PLL and Clock Signals                                  |               | 5                 | <b>Table 2-4</b>     |
| Interrupt and Mode Control                             |               | 5                 | <b>Table 2-5</b>     |
| External Memory Interface (also referred to as Port A) | Address Bus   | 16                | <b>Table 2-6</b>     |
|                                                        | Data Bus      | 24                |                      |
|                                                        | Bus Control   | 4                 |                      |
| Host Interface (HI08)                                  | Port B (GPIO) | 16                | <b>Table 2-8</b>     |
| Synchronous Serial Interface 0 (SSI0)                  | Port C (GPIO) | 6                 | <b>Table 2-9</b>     |
| Synchronous Serial Interface 1 (SSI1)                  | Port D (GPIO) | 6                 | <b>Table 2-10</b>    |
| General Purpose Input/Output (GPIO)                    |               | 3                 | <b>Table 2-11</b>    |
| Triple Timer                                           |               | 3                 | <b>Table 2-12</b>    |
| JTAG Interface/On-Chip Emulation (OnCE) Module         |               | 6                 | <b>Table 2-13</b>    |

# Freescale Semiconductor, Inc.

## Signal/Connection Description

### Introduction

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- Note:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each these modes is configured independently, any combination of these modes is possible. The HI08 signals can also be configured alternately as GPIO signals (PB0-PB15).
  2. The SSI0 and SSI1 signals can be configured alternately as Port C GPIO signals (PC0-PC5) and Port D GPIO signals (PD0-PD5), respectively.
  3. TIO0-TIO2 can be configured alternately as GPIO signals.

AA1097

**Figure 2-1 DSP56602 Signals Identified by Functional Group**

## 2.2 POWER

Table 2-2 Power Inputs

| Signal Name<br>(no. of pins) | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>CCA</sub> (3)         | <b>Address Bus Power</b> —V <sub>CCA</sub> is an isolated power for sections of address bus I/O drivers, and must be tied externally to all other chip power inputs, except for the V <sub>CCQL</sub> input. The user must provide adequate external decoupling capacitors.                                                                                                                                                                                  |
| V <sub>CCC</sub> (1)         | <b>Bus Control Power</b> —V <sub>CCC</sub> is an isolated power for the bus control I/O drivers, and must be tied to all other chip power inputs externally, except for the V <sub>CCQL</sub> input. The user must provide adequate external decoupling capacitors.                                                                                                                                                                                          |
| V <sub>CCD</sub> (4)         | <b>Data Bus Power</b> —V <sub>CCD</sub> is an isolated power for sections of data bus I/O drivers, and must be tied to all other chip power inputs externally, except for the V <sub>CCQL</sub> input. The user must provide adequate external decoupling capacitors.                                                                                                                                                                                        |
| V <sub>CCH</sub> (1)         | <b>Host Power</b> —V <sub>CCH</sub> is an isolated power for the HI08 logic, and must be tied to all other chip power inputs externally, except for the V <sub>CCQL</sub> input. The user must provide adequate external decoupling capacitors.                                                                                                                                                                                                              |
| V <sub>CCP</sub> (1)         | <b>PLL Power</b> —V <sub>CCP</sub> is V <sub>CC</sub> dedicated for Phase Lock Loop (PLL) use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V <sub>CC</sub> power rail.                                                                                                                                                                                                                 |
| V <sub>CCQH</sub> (3)        | <p><b>Quiet Power High Voltage</b>—V<sub>CCQH</sub> is an isolated power for the CPU logic, and must be tied to all other chip power inputs externally, except for the V<sub>CCQL</sub> input. The user must provide adequate external decoupling capacitors.</p> <p>The voltage supplied to these inputs should equal the voltage supplied to I/O power inputs V<sub>CCA</sub>, V<sub>CCC</sub>, V<sub>CCD</sub>, V<sub>CCH</sub>, and V<sub>CCS</sub>.</p> |
| V <sub>CCQL</sub> (4)        | <b>Quiet Power Low Voltage</b> —V <sub>CCQL</sub> is an isolated power for the CPU logic, and should not be tied to the other chip power inputs. The user must provide adequate external decoupling capacitors.                                                                                                                                                                                                                                              |
| V <sub>CCS</sub> (2)         | <b>SSI, GPIO, and Timers Power</b> —V <sub>CCS</sub> is an isolated power for the SSIs, GPIO, and Timers logic, and must be tied to all other chip power inputs externally, except for the V <sub>CCQL</sub> inputs. The user must provide adequate external decoupling capacitors.                                                                                                                                                                          |

## 2.3 GROUND

**Table 2-3** Grounds

| Signal Name<br>(no. of pins) | Signal Description                                                                                                                                                                                                                                                            |
|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND <sub>A</sub> (4)         | <b>Address Bus Ground</b> —GND <sub>A</sub> is an isolated ground for sections of address bus I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                   |
| GND <sub>C</sub> (2)         | <b>Bus Control Ground</b> —GND <sub>C</sub> is an isolated ground for the bus control I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                           |
| GND <sub>D</sub> (4)         | <b>Data Bus Ground</b> —GND <sub>D</sub> is an isolated ground for sections of the data bus I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                     |
| GND <sub>H</sub> (1)         | <b>Host Ground</b> —GND <sub>H</sub> is an isolated ground for the HI08 I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                                         |
| GND <sub>P</sub> (1)         | <b>PLL Ground</b> —GND <sub>P</sub> is ground dedicated for PLL use, and should be provided with an extremely low impedance path to ground. V <sub>CCP</sub> should be bypassed to GND <sub>P</sub> with a 0.1 μF capacitor located as close as possible to the chip package. |
| GND <sub>P1</sub> (1)        | <b>PLL Ground 1</b> —GND <sub>P1</sub> is ground dedicated for PLL use, and should be provided with an extremely low impedance path to ground.                                                                                                                                |
| GND <sub>Q</sub> (4)         | <b>Quiet Ground</b> —GND <sub>Q</sub> is an isolated ground for the CPU logic, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                                               |
| GND <sub>S</sub> (2)         | <b>SSIs, GPIO, and Timers Ground</b> —GNDS is an isolated ground for the SSIs, GPIO, and Timers logic, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.                                       |

## 2.4 CLOCK AND PHASE LOCK LOOP

Table 2-4 Clock and PLL Signals

| Signal Name             | Signal Type | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                    |
|-------------------------|-------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EXTAL                   | Input       | Input              | <b>External Clock/Crystal Input</b> —EXTAL interfaces the internal crystal oscillator input to an external crystal or an external clock.                                                                                                                                                                                                                              |
| XTAL                    | Output      | Chip-driven        | <b>Crystal Output</b> —XTAL connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.                                                                                                                                                                                                             |
| PCAP                    | Input       | Indeterminate      | <p><b>PLL Capacitor</b>—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V<sub>CCP</sub>.</p> <p>If the PLL is not used, PCAP may be tied to V<sub>CC</sub>, GND, or left floating.</p>                                                                                          |
| CLKOUT                  | Output      | Chip-driven        | <p><b>Clock Output</b>—CLKOUT provides an output clock synchronized to the internal core clock phase. When the PLL is enabled, the Division Factor (DF) equals one, and the Multiplication Factor (MF) is less than or equal to four, CLKOUT is also synchronized to EXTAL.</p> <p>When the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.</p> |
| PINIT                   | Input       | Input              | <b>PLL Initialize</b> —During assertion of $\overline{\text{RESET}}$ , the value of PINIT is written into the PLL Enable (PEN) bit of the PLL Control Register 1 (PCTL1), determining whether the PLL is enabled or disabled. When this input is high during $\overline{\text{RESET}}$ assertion, the PLL is enabled following $\overline{\text{RESET}}$ deassertion. |
| $\overline{\text{NMI}}$ | Input       |                    | <p><b>Non-Maskable Interrupt</b>—After <math>\overline{\text{RESET}}</math> deassertion and during normal instruction processing, the <math>\overline{\text{NMI}}</math> Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT.</p> <p>This input can tolerate 5 V.</p>                           |

## 2.5 INTERRUPT AND MODE CONTROL

**Table 2-5** Interrupt and Mode Control Signals

| Signal Name | Signal Type | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------|-------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RESET       | Input       | Input              | <p><b>Reset</b>—RESET is an active low, Schmitt-trigger input. Deassertion of the RESET signal is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input, such as a capacitor charging, to reliably reset the chip. If the RESET signal is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start up synchronously and operate together. When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs.</p> <p>This input can tolerate 5 V.</p> |
| MODA        | Input       | Input              | <p><b>Mode Select A</b>—MODA selects the initial chip operating mode during hardware reset. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the Operating Mode Register (OMR) when the RESET signal is deasserted.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| IRQA        | Input       |                    | <p><b>External Interrupt Request A</b>—Following RESET deassertion, MODA becomes IRQA, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If IRQA is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting IRQA to exit the Wait state. If the processor is in the Stop standby state and IRQA is asserted, the processor exits the Stop state.</p> <p>This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.</p>                                                                                                                |

**Table 2-5** Interrupt and Mode Control Signals (continued)

| Signal Name              | Signal Type | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------|-------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MODB                     | Input       | Input              | <p><b>Mode Select B</b>—MODB selects the initial chip operating mode during hardware reset. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the OMR when the <math>\overline{\text{RESET}}</math> signal is deasserted.</p>                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{IRQB}}$ | Input       |                    | <p><b>External Interrupt Request B</b>—Following <math>\overline{\text{RESET}}</math> deassertion, MODB becomes <math>\overline{\text{IRQB}}</math>, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If <math>\overline{\text{IRQB}}</math> is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting <math>\overline{\text{IRQB}}</math> to exit the Wait state.</p> <p>This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.</p> |
| MODC                     | Input       | Input              | <p><b>Mode Select C</b>—MODC selects the initial chip operating mode during hardware reset. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the OMR when the <math>\overline{\text{RESET}}</math> signal is deasserted.</p>                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{IRQC}}$ | Input       |                    | <p><b>External Interrupt Request C</b>—Following <math>\overline{\text{RESET}}</math> deassertion, MODC becomes <math>\overline{\text{IRQC}}</math>, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If <math>\overline{\text{IRQC}}</math> is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting <math>\overline{\text{IRQC}}</math> to exit the Wait state.</p> <p>This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.</p> |

Table 2-5 Interrupt and Mode Control Signals (continued)

| Signal Name                                                                                   | Signal Type | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------------------------------------------------------------|-------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MODD                                                                                          | Input       | Input              | <b>Mode Select D</b> —MODD selects the initial chip operating mode during hardware reset. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted.                                                                                                                                                                                                                                                                                                                                                                      |
| $\overline{\text{IRQD}}$                                                                      | Input       |                    | <p><b>External Interrupt Request C</b>—Following <math>\overline{\text{RESET}}</math> deassertion, MODD becomes <math>\overline{\text{IRQD}}</math>, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If <math>\overline{\text{IRQD}}</math> is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting <math>\overline{\text{IRQD}}</math> to exit the Wait state.</p> <p>This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.</p> |
| Note: See also PINIT/ $\overline{\text{NMI}}$ in Table 2-4 Clock and PLL Signals on page 2-7. |             |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

## 2.6 EXTERNAL MEMORY INTERFACE (PORT A)

Table 2-6 External Memory Interface (Port A) Signals

| Signal Name             | Signal Type  | State During Reset                    | Signal Description                                                                                                                                                                                                              |
|-------------------------|--------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0–A15                  | Output       | Set according to chip operating mode* | <b>Address Bus</b> —These active high outputs specify the address for external program memory accesses. To minimize power dissipation, A0–A15 do not change state when external memory spaces are not being accessed.           |
| D0–D23                  | Input/Output | Tri-stated                            | <b>Data Bus</b> —These active high, bidirectional input/outputs provide the bidirectional data bus for external program memory accesses. D0–D23 are tri-stated when no external bus activity occurs, and during hardware reset. |
| $\overline{\text{MCS}}$ | Output       | Pulled high internally                | <b>Memory Chip Select</b> —This signal is an active low output, and is asserted when an external memory access occurs. $\overline{\text{MCS}}$ is deasserted during hardware reset.                                             |

**Table 2-6** External Memory Interface (Port A) Signals (continued)

| Signal Name     | Signal Type                                                                                                                                                                                                                                                                                                                                                | State During Reset     | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{RD}$ | Output                                                                                                                                                                                                                                                                                                                                                     | Pulled high internally | <b>Read Enable</b> —This signal is an active low output. $\overline{RD}$ is asserted to read external memory on the data bus (D0–D23). $\overline{RD}$ is deasserted during hardware reset.                                                                                                                                                                                                                                           |
| $\overline{WR}$ | Output                                                                                                                                                                                                                                                                                                                                                     | Pulled high internally | <b>Write Enable</b> —This signal is an active low output. $\overline{WR}$ is asserted to write external memory on the data bus (D0–D23). $\overline{WR}$ is deasserted during hardware reset.                                                                                                                                                                                                                                         |
| $\overline{AT}$ | Output                                                                                                                                                                                                                                                                                                                                                     | Pulled high internally | <b>Address Tracing</b> —This signal is an active low output. $\overline{AT}$ is asserted (for half of a clock cycle) whenever a new address is driven on the address bus (A0–A15) in the Program Address Tracing mode. The new address is either a reflection of internal fetch or internal program space move instruction or an external address driven for an external access. $\overline{AT}$ is deasserted during hardware reset. |
| Note:           | * The A0–A15 pins are asserted according to the selected chip operating mode, as determined by the values on the MODA–MODD pins. Each mode has a different reset address. A0–A15 are latched to the value of that reset address minus 1. For example, if the reset address for a selected operating mode is \$0800, the address bus is asserted to \$07FF. |                        |                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## 2.7 HOST INTERFACE (HI08)

The HI08 provides a fast 8-bit port that can be connected directly to the host bus. The HI08 supports a variety of standard buses, and can be directly connected to a number of industry-standard microcomputers, microprocessors, and DSPs.

### 2.7.1 Host Port Usage Considerations

Careful synchronization is required when reading multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in the following table:

**Table 2-7** Host Port Usage Considerations

| Action                                        | Description                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Asynchronous read of receive byte registers   | When reading the receive byte registers, Receive High (RXH) register or Receive Low (RXL) register, the Host Interface programmer should use interrupts or poll the Receive Register Data Full (RXDF) flag, which indicates that data is available. This assures that the data in the receive byte registers is valid.                                                      |
| Asynchronous write to transmit byte registers | The host interface programmer should not write to the transmit byte registers, Transmit High (TXH) register or Transmit Low (TXL) register, unless the Transmit Register Data Empty (TXDE) bit is set, which indicates that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register. |
| Asynchronous write to host vector             | The Host Interface programmer should change the Host Vector (HV) register only when the Host Command (HC) bit is clear. This guarantees that the DSP interrupt control logic receives a stable vector.                                                                                                                                                                      |

### 2.7.2 Host Port Configuration

The signal functions associated with the HI08 vary according to the configuration determined by the HI08 Port Control Register (HPCR). Refer to **Section 7, Host Interface (HI08)**, for detailed descriptions of this and the other configuration registers used with the HI08.

**Table 2-8** Host Interface Signals

| Signal Name                  | Signal Type     | State During Reset              | Signal Description                                                                                                                                                                                                                                                                                                                                                 |
|------------------------------|-----------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HD0–HD7                      | Bi-directional  | Discon-<br>nected<br>internally | <b>Host Data Bus</b> —When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Host Data bidirectional tri-state bus (HD0–HD7).                                                                                                                                                     |
| HAD0–HAD7                    | Bi-directional  |                                 | <b>Host Address and Data Bus</b> —When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Host Address/Data multiplexed bidirectional tri-state bus (HAD0–HAD7).                                                                                                                       |
| PB0–PB7                      | Input or Output |                                 | <p><b>Port B 0–7</b>—When the HI08 is configured as GPIO through the HI08 Port Control Register (HPCR), these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register (HDDR).</p> <p>When configured as an input, these pins can tolerate 5 V. These pins are electrically disconnected internally during Stop mode.</p> |
| HA0                          | Input           | Discon-<br>nected<br>internally | <b>Host Address Input 0</b> —When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 0 of the Host Address input bus (HA0).                                                                                                                                                                       |
| $\overline{\text{HAS}}$ /HAS | Input           |                                 | <b>Host Address Strobe</b> —When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the Host Address Strobe ( $\overline{\text{HAS}}$ ) Schmitt-trigger input. The polarity of the address strobe is programmable.                                                                                         |
| PB8                          | Input or Output |                                 | <p><b>Port B 8</b>—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                                      |

**Table 2-8** Host Interface Signals (continued)

| Signal Name | Signal Type        | State During Reset              | Signal Description                                                                                                                                                                                                                                                                             |
|-------------|--------------------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HA1         | Input              | Discon-<br>nected<br>internally | <b>Host Address Input 1</b> —When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line one of the Host Address input bus (HA1).                                                                                                 |
| HA8         | Input              |                                 | <b>Host Address 8</b> —When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line eight of the input Host Address bus (HA8).                                                                                                         |
| PB9         | Input or<br>Output |                                 | <p><b>Port B 9</b>—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>  |
| HA2         | Input              | Discon-<br>nected<br>internally | <b>Host Address Input 2</b> —When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line two of the Host Address input bus (HA2).                                                                                                 |
| HA9         | Input              |                                 | <b>Host Address 9</b> —When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line nine of the input Host Address bus (HA9).                                                                                                          |
| PB10        | Input or<br>Output |                                 | <p><b>Port B 10</b>—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |

Table 2-8 Host Interface Signals (continued)

| Signal Name                      | Signal Type     | State During Reset      | Signal Description                                                                                                                                                                                                                                                                       |
|----------------------------------|-----------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HRW                              | Input           | Disconnected internally | <b>Host Read/Write</b> —When the HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Read/Write input (HRW).                                                                                                               |
| $\overline{\text{HRD}}$ /<br>HRD | Input           |                         | <b>Host Read Data</b> —When the HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Read Data strobe Schmitt-trigger input ( $\overline{\text{HRD}}$ ). The polarity of the data strobe is programmable.                   |
| PB11                             | Input or Output |                         | <b>Port B 11</b> —When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode. |
| $\overline{\text{HDS}}$ /HDS     | Input           | Disconnected internally | <b>Host Data Strobe</b> —When the HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Data Strobe Schmitt-trigger input ( $\overline{\text{HDS}}$ ). The polarity of the data strobe is programmable.                 |
| $\overline{\text{HWR}}$ /<br>HWR | Input           |                         | <b>Host Write Enable</b> —When the HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Write Data Strobe Schmitt-trigger input ( $\overline{\text{HWR}}$ ). The polarity of the data strobe is programmable.               |
| PB12                             | Input or Output |                         | <b>Port B 12</b> —When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode. |

**Table 2-8** Host Interface Signals (continued)

| Signal Name                        | Signal Type        | State During Reset              | Signal Description                                                                                                                                                                                                                                                                                                                                        |
|------------------------------------|--------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HCS/HCS                            | Input              | Discon-<br>nected<br>internally | <b>Host Chip Select</b> —When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is the Host Chip Select input ( $\overline{\text{HCS}}$ ). The polarity of the chip select is programmable.                                                                                                     |
| HA10                               | Input              |                                 | <b>Host Address 10</b> —When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the input Host Address bus (HA10).                                                                                                                                                                     |
| PB13                               | Input or<br>Output |                                 | <b>Port B 13</b> —When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.                                                                  |
| $\overline{\text{HREQ}}$ /<br>HREQ | Output             | Discon-<br>nected<br>internally | <b>Host Request</b> —When the HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Request output ( $\overline{\text{HREQ}}$ ). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output.                                 |
| $\overline{\text{HTRQ}}$ /<br>HTRQ | Output             |                                 | <b>Transmit Host Request</b> —When the HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Transmit Host Request output ( $\overline{\text{HTRQ}}$ ). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output.               |
| PB14                               | Input or<br>Output |                                 | <b>Port B 14</b> —When the HI08 is programmed to interface a multiplexed host bus and the signal is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode. |

Table 2-8 Host Interface Signals (continued)

| Signal Name                          | Signal Type     | State During Reset      | Signal Description                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------|-----------------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{HACK}}/\text{HACK}$ | Input           | Disconnected internally | <b>Host Acknowledge</b> —When the HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Acknowledge Schmitt-trigger input ( $\overline{\text{HACK}}$ ). The polarity of the host acknowledge is programmable.                                                           |
| $\overline{\text{HRRQ}}/\text{HRRQ}$ | Output          |                         | <b>Receive Host Request</b> —When the HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Receive Host Request output ( $\overline{\text{HRRQ}}$ ). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output. |
| PB15                                 | Input or Output |                         | <b>Port B 15</b> —When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.                                                  |

## 2.8 SYNCHRONOUS SERIAL INTERFACE 0 (SSI0)

Two identical Synchronous Serial Interfaces (SSI0 and SSI1) provide a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, or microprocessors. When either SSI port is disabled, it can be used for General Purpose I/O (GPIO).

**Table 2-9** Synchronous Serial Interface 0 (SSI0)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                      |
|-------------|-----------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SC00        | Input or Output | Input              | <b>Serial Control Signal 0</b> —The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for or for Serial I/O Flag 0.                                                                   |
| PC0         | Input or Output |                    | <p><b>Port C 0</b>—When configured as PC0, signal direction is controlled through the SSI0 Port Direction Control Register (PRRC). The signal can be configured as SSI signal SC00 through the SSI0 Port Control Register (PCRC).</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| SC01        | Input or Output | Input              | <b>Serial Control Signal 1</b> —The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for Serial I/O Flag 1.                                                                          |
| PC1         | Input or Output |                    | <p><b>Port C 1</b>—When configured as PC1, signal direction is controlled through the PRRRC register. The signal can be configured as an SSI signal SC01 through the PCRC register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                               |

**Table 2-9** Synchronous Serial Interface 0 (SSI0) (continued)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------|-----------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SC02        | Input or Output | Input              | <b>Serial Control Signal 2</b> —SC02 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).                                                                                                                                                                                                               |
| PC2         | Input or Output |                    | <p><b>Port C 2</b>—When configured as PC2, signal direction is controlled through the PRRC register. The signal can be configured as an SSI signal SC02 through the PCRC register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                                                                                                                                                                                                                                                                     |
| SCK0        | Input or Output | Input              | <p><b>Serial Clock</b>—SCK0 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the SSI. The SCK0 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes.</p> <p>Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external SSI clock frequency). The SSI needs at least three DSP phases inside each half of the serial clock.</p> |
| PC3         | Input or Output |                    | <p><b>Port C 3</b>—When configured as PC3, signal direction is controlled through the PRRC register. The signal can be configured as an SSI signal SCK0 through the PCRC register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                                                                                                                                                                                                                                                                     |

**Table 2-9** Synchronous Serial Interface 0 (SSI0) (continued)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                        |
|-------------|-----------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRD0        | Input           | Input              | <b>Serial Receive Data</b> —SRD0 receives serial data and transfers the data to the SSI receive shift register. SRD0 is an input when data is being received.                                                                                                                                                             |
| PC4         | Input or Output |                    | <p><b>Port C 4</b>—When configured as PC4, signal directions is controlled through the PRRC register. The signal can be configured as an SSI signal SRD0 through the PCRC register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| STD0        | Output          | Input              | <b>Serial Transmit Data</b> —STD0 is used for transmitting data from the serial transmit shift register. STD0 is an output when data is being transmitted.                                                                                                                                                                |
| PC5         | Input or Output |                    | <p><b>Port C 5</b>—When configured as PC5, signal directions is controlled through the PRRC register. The signal can be configured as an SSI signal STD0 through the PCRC register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |

## 2.9 SYNCHRONOUS SERIAL INTERFACE 1 (SSI1)

**Table 2-10** Synchronous Serial Interface 1 (SSI1)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                      |
|-------------|-----------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SC10        | Input or Output | Input              | <b>Serial Control Signal 0</b> —The function of SC10 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for or for Serial I/O Flag 0.                                                                   |
| PD0         | Input or Output |                    | <p><b>Port D 0</b>—When configured as PD0, signal direction is controlled through the SSI1 Port Direction Control Register (PRRD). The signal can be configured as SSI signal SC10 through the SSI1 Port Control Register (PCRD).</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| SC11        | Input or Output | Input              | <b>Serial Control Signal 1</b> —The function of SC11 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for Serial I/O Flag 1.                                                                          |
| PD1         | Input or Output |                    | <p><b>Port D 1</b>—When configured as PD1, signal direction is controlled through the PRRD register. The signal can be configured as an SSI signal SC11 through the PCRD register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                |

**Table 2-10** Synchronous Serial Interface 1 (SSI1) (continued)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------|-----------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SC12        | Input or Output | Input              | <p><b>Serial Control Signal 2</b>—SC12 is used for frame sync I/O. SC12 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).</p>                                                                                                                                                                        |
| PD2         | Input or Output |                    | <p><b>Port D 2</b>—When configured as PD2, signal direction is controlled through the PRRD register. The signal can be configured as an SSI signal SC12 through the PCRD register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                                                                                                                                                                                                                                                                     |
| SCK1        | Input or Output | Input              | <p><b>Serial Clock</b>—SCK1 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the SSI. The SCK1 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes.</p> <p>Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external SSI clock frequency). The SSI needs at least three DSP phases inside each half of the serial clock.</p> |
| PD3         | Input or Output |                    | <p><b>Port D 3</b>—When configured as PD3, signal direction is controlled through the PRRD register. The signal can be configured as an SSI signal SCK1 through the PCRD register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p>                                                                                                                                                                                                                                                                                                     |

Table 2-10 Synchronous Serial Interface 1 (SSI1) (continued)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                       |
|-------------|-----------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRD1        | Input           | Input              | <b>Serial Receive Data</b> —SRD1 receives serial data and transfers the data to the SSI Receive Shift Register.                                                                                                                                                                                                          |
| PD4         | Input or Output |                    | <p><b>Port D 4</b>—When configured as PD4, signal direction is controlled through the PRRD register. The signal can be configured as an SSI signal SRD1 through the PCRD register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| STD1        | Input           | Input              | <b>Serial Transmit Data</b> —STD1 is used for transmitting data from the SSI Transmit Shift Register.                                                                                                                                                                                                                    |
| PD5         | Input or Output |                    | <p><b>Port D 5</b>—When configured as PD5, signal direction is controlled through the PRRD register. The signal can be configured as an SSI signal STD1 through the PCRD register.</p> <p>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |

## 2.10 GENERAL PURPOSE I/O (GPIO)

Three dedicated General Purpose Input/Output (GPIO) signals are provided on the DSP56602. Each is reconfigurable as input, output, or tri-state. These signals are exclusively defined as GPIO, and do not offer additional functionality.

**Table 2-11** General Purpose I/O (GPIO)

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                         |
|-------------|-----------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO0       | Input or Output | Input              | <p><b>General Purpose I/O 0</b>—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software.</p> <p>This input can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| GPIO1       | Input or Output | Input              | <p><b>General Purpose I/O 1</b>—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software.</p> <p>This input can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |
| GPIO2       | Input or Output | Input              | <p><b>General Purpose I/O 2</b>—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software.</p> <p>This input can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.</p> |

## 2.11 TRIPLE TIMER

Three identical and independent timers are implemented. The three timers can use internal or external clocking and can interrupt the DSP after a specified number of events (clocks), or can signal an external device after counting a specific number of internal events. When a timer port is disabled, it can be used for General Purpose I/O (GPIO).

**Table 2-12** Triple Timer Signals

| Signal Name | Signal Type     | State During Reset | Signal Description                                                                                                                                                                                                                                                                              |
|-------------|-----------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TIO0        | Input or Output | GPIO Input         | <b>Timer 0 Schmitt-Trigger Input/Output</b> —When TIO0 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO0 is used as an output, the timer module functions as a timer and TIO0 provides the timer pulse. |
|             | Input or Output |                    | When TIO0 is not used by the timer module, it can be used for GPIO.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.                                                                                           |
| TIO1        | Input or Output | GPIO Input         | <b>Timer 1 Schmitt-Trigger Input/Output</b> —When TIO1 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO1 is used as an output, the timer module functions as a timer and TIO1 provides the timer pulse. |
|             | Input or Output |                    | When TIO1 is not used by the timer module, it can be used for GPIO.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.                                                                                           |
| TIO2        | Input or Output | GPIO Input         | <b>Timer 2 Schmitt-Trigger Input/Output</b> —When TIO2 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO2 is used as an output, the timer module functions as a timer and TIO2 provides the timer pulse. |
|             | Input or Output |                    | When TIO2 is not used by the timer module, it can be used for GPIO.<br><br>When configured as an input, this pin can tolerate 5 V. This pin is electrically disconnected internally during Stop mode.                                                                                           |

## 2.12 JTAG/ONCE INTERFACE

**Table 2-13** JTAG Interface/On-Chip Emulation Module (OnCE) Signals

| Signal Name              | Signal Type    | State During Reset | Signal Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------|----------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TCK                      | Input          | Input              | <p><b>Test Clock</b>—TCK is a test clock input signal used to synchronize the JTAG test logic. The TCK pin can be tri-stated.</p> <p>This input can tolerate 5 V.</p>                                                                                                                                                                                                                                                                         |
| TDI                      | Input          | Input              | <p><b>Test Data Input</b>—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of the TCK signal and has an internal pull-up resistor.</p> <p>This input can tolerate 5 V.</p>                                                                                                                                                                                                       |
| TDO                      | Output         | Tri-stated         | <p><b>Test Data Output</b>—TDO is a test data serial output signal used for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of the TCK signal.</p>                                                                                                                                                                                    |
| TMS                      | Input          | Input              | <p><b>Test Mode Select</b>—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of the TCK signal and has an internal pull-up resistor.</p> <p>This input can tolerate 5 V.</p>                                                                                                                                                                                                     |
| $\overline{\text{TRST}}$ | Input          | Input              | <p><b>Test Reset</b>—<math>\overline{\text{TRST}}</math> is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. <math>\overline{\text{TRST}}</math> has an internal pull-up resistor. <math>\overline{\text{TRST}}</math> must be asserted after power up.</p> <p>This input can tolerate 5 V.</p>                                                                                              |
| $\overline{\text{DE}}$   | Bi-directional | Input              | <p><b>Debug Event</b>—<math>\overline{\text{DE}}</math> is an open-drain bidirectional active-low signal providing, as an input, a means of entering the Debug mode of operation from an external command controller, and as an output, a means of acknowledging that the chip has entered the Debug mode. The <math>\overline{\text{DE}}</math> has an internal pull-up resistor.</p> <p>When this pin is an input, it can tolerate 5 V.</p> |

